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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/635,945	08/10/2000	Setsuo Nakajima	SEL 203	5934
7590 05/25/2005			EXAMINER	
Cook Alex McFarron Manzo Cummings & Mehler LTD			HU, SHOUXIANG	
Suite 2850			ART UNIT	
200 West Adams Street			PAPER NUMBER	
Chicago, IL 60606			2811	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/635,945

Applicant(s)

NAKAJIMA ET AL.

Examiner

Shouxiang Hu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 February 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 26-28 and 30-42 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 26-28 and 30-42 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: A thin film transistor device with a contact terminal.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 26-28 and 30-42 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claims 26, 27, 28 and 30-34 each recite the subject matter that an edge of the second layer of the input terminal portion is aligned with an edge of the substrate; but the original disclosure lacks an adequate description on it, especially regarding which edge of the second layer of the input terminal portion is aligned with which edge of the substrate. Applicant's remarks filed on February 15, 2005 contend that support for such subject matters can be found in Figs. 4

A and 4B and on Pages 22-23 of the specification. However, Figs. 4A and 4B are indeed truncated drawings, in which the width of the substrate is truncated, so as to show only one TFT or pixel cell; and, no real edges of the substrate are shown there. No adequate description on such subject matters can be found on Pages 22-23 of the specification, either.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 31-34, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Shin (US 5,825,449).

Shin discloses a semiconductor device (Figs. 1a-1f; also see col. 1, lines 34-67), comprising: a substrate (1; glass); a thin film transistor comprising a gate electrode (2), a first insulating layer over the gate electrode, a channel forming region in an amorphous semiconductor layer (4), and doped source and drain regions (5); a second interlayer insulating layer (9; nitride, inorganic); a pixel electrode (6); a storage capacitor wiring ("20" and/or "2D"); and, a source input terminal portion (a source pad, also see the top row pads 640 in Fig. 6) including a first layer (2A) comprising the same material as that of the gate electrode (2) and a second layer (6A) comprising the same material as that of the pixel electrode in contact with the first layer through a contact hole formed

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in the first insulating layer, wherein the gate electrode, the storage capacitor wiring layer and the first layer in the input terminal portion all have a tapered shape and are formed from a same conductive layer; and the storage capacitor wiring and a portion of the pixel electrode, with a portion of the first insulating layer disposed therebetween, inherently form a storage capacitor. And, the device further comprises a source wiring (7; also see source wiring 610 in Fig. 6), wherein a portion of the wiring (7) is formed over the source region (left side of film 5) and another portion of the source (7) is formed on the second layer (6A) of the source input terminal portion. Furthermore, it is noted that the second layer (6A) in the source input terminal portion (also see the top row source input pads in Fig. 6) naturally has an edge that is aligned with an side edge of the substrate, as the source pad is formed with the second layer, and is rectangle-shaped (see Fig. 6) with its edges naturally respectively parallel with the major edges of substrate that comprises the actively-addressed display matrix thereon. And, it is also noted that the second insulating layer (9) in Shin naturally overlaps with a portion of the pixel electrode (6), as the second insulating layer (9) therein overlaps with at least a portion of the pixel electrode (6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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3. Claims 39-42, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin.

The disclosure of Shin is discussed as applied to claims 31-34 above.

Although Shin does not expressly disclose that the device can be applied in one of the selected applications as recited in these claims, each of these recited application are art-known applications for an LCD device such as the one of Shin, in order to achieve better display performance with reduced size, as readily evidenced in the prior art such as Ikeda et al. (US 5,428,250; see col.1, lines 16-24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device of Shin and applied it to one of the art-known applications, so that a better display performance in the application with reduced size would be obtained.

4. Claims 26-28, 30 and 35-38, insofar as being in compliance with 35 U.S.C. 112 and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin in view of Ikeda et al. ("Ikeda"; US 5,428,250).

The disclosure of Shin is discussed as applied to claim 31-34 and 39-42 above.

Although Shin does not expressly disclose that the storage wiring can be completely covered by the pixel electrode, one of ordinary skill in the art would readily recognize that the storage wiring can be completely covered by the pixel electrode for

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enhancing the storage capacitance therebetween, as evidenced in Ikeda (see the capacitor line 6 and the pixel electrode 10 in Figs. 6-12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the semiconductor device of Shin with the storage wiring being completely covered by the pixel electrode, as taught in Ikeda, so that an LCD device with enhanced storage capacitance would be obtained.

Response to Arguments

Applicant's arguments filed on February 15, 2005, have been fully considered but they are not persuasive.

Applicant's main arguments include: the applied prior art references fail to teach the recited feature regarding the edge alignment. Responses to these arguments have been fully incorporated into the claim rejections under 35 U.S.C 112, 102 and 103 set forth above in this Office action. Furthermore, it is noted that the second layer (6A) in the source input terminal portion (also see the top row source input pads in Fig. 6) naturally has an edge that is aligned with an side edge of the substrate, as the source pad is formed with the second layer, and is rectangle-shaped (see Fig. 6) with its edges naturally respectively parallel with the major edges of substrate that comprises the actively-addressed display matrix thereon, as such matrix type display screen along with the underlying substrate is commonly rectangle-shaped.

In addition, the second insulating layer (9) in Shin naturally overlaps with a portion of the pixel electrode (6), as the second insulating layer (9) therein overlaps with at least a portion of the pixel electrode (6).

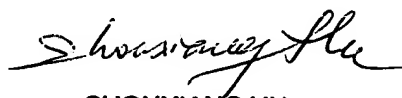
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
May 23, 2005


SHOUXIANG HU
PRIMARY EXAMINER